SPACE CODESIGN

Dynamic virtual platform for HW/SW partitioning on MPSoC platforms

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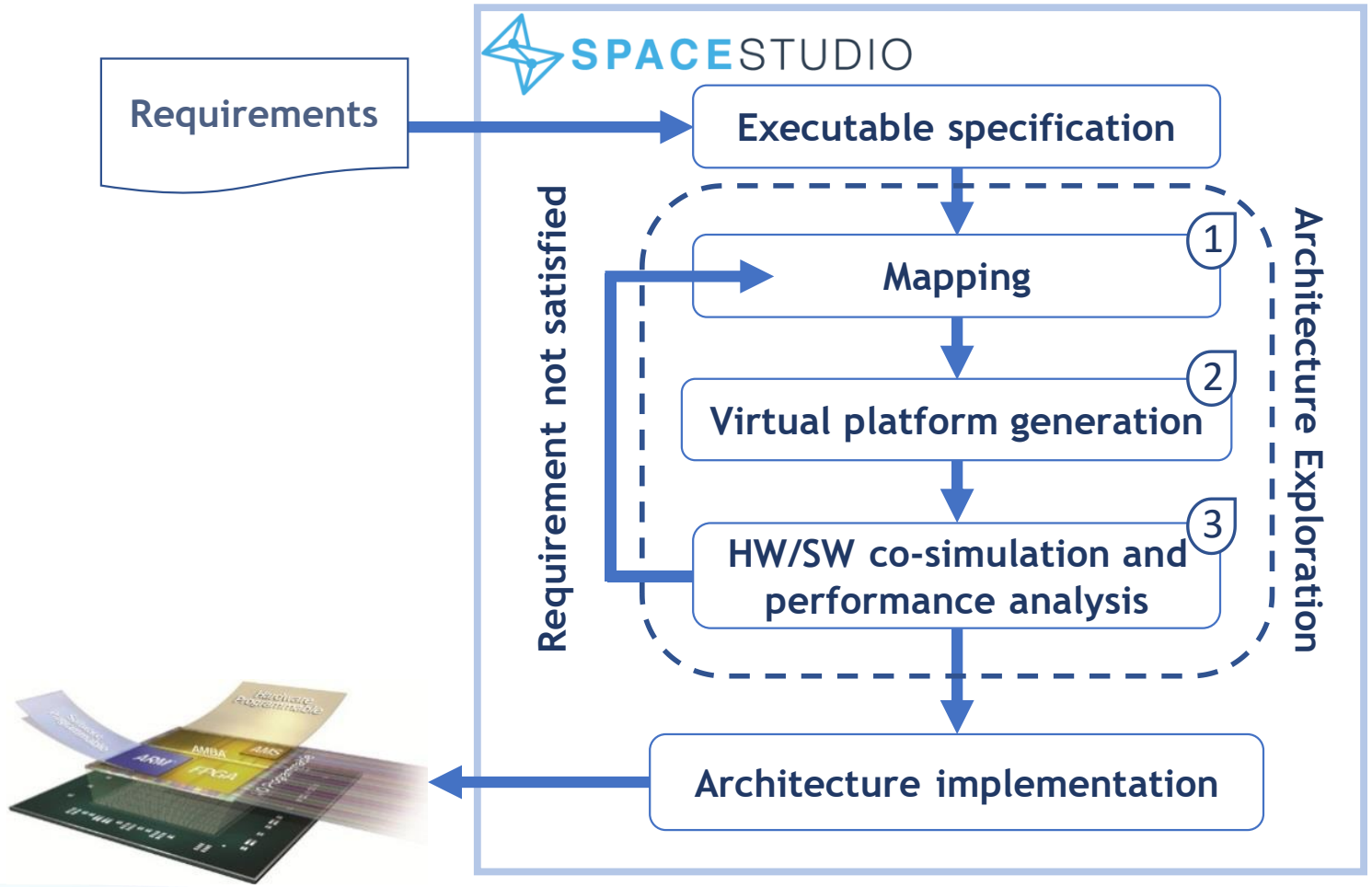
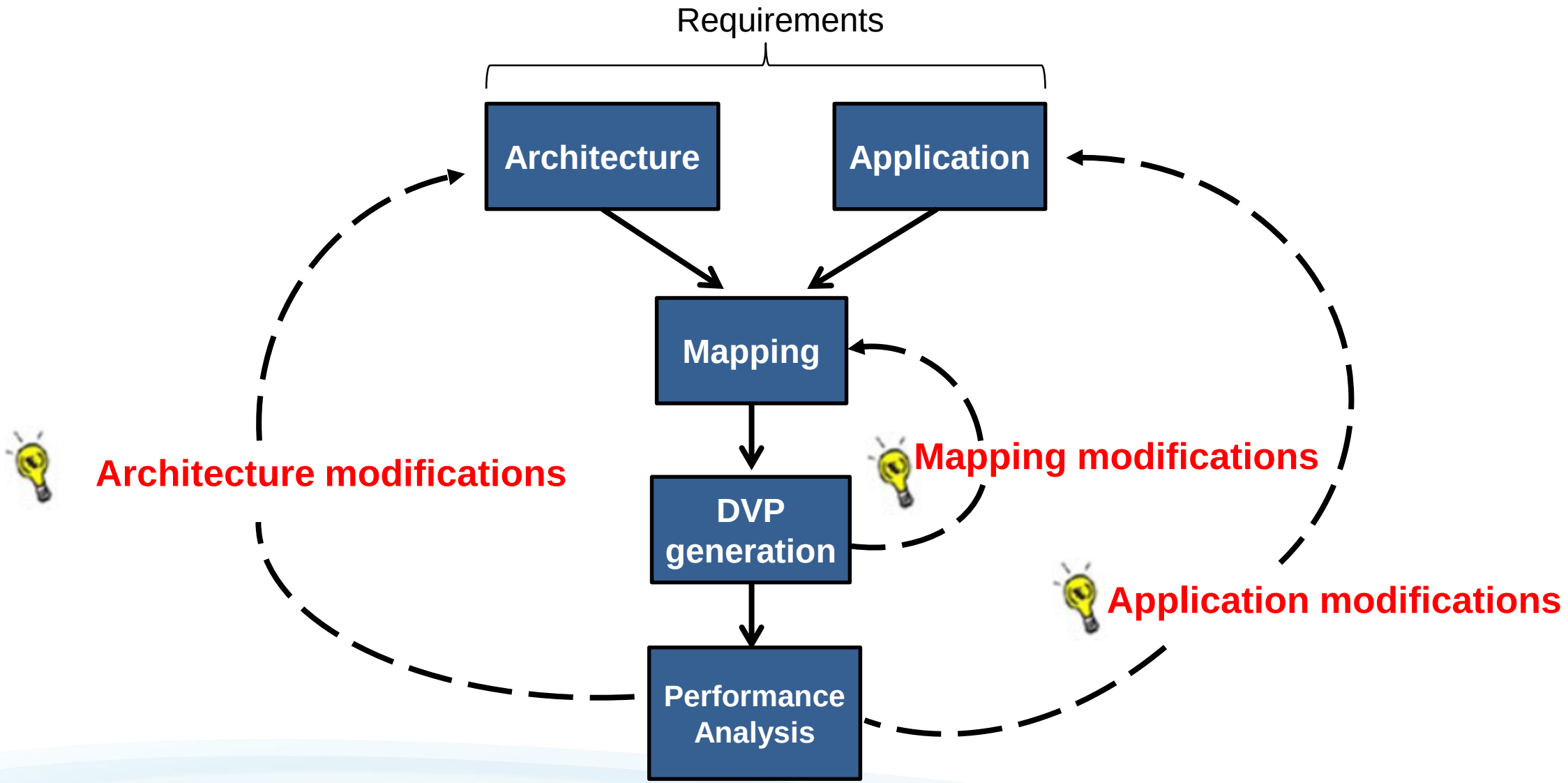
Overview of SpaceStudio

3-steps methodology driven by the application



Dynamic Virtual Platform (DVP) & Architectural Exploration



Performance Analysis Results

- **Zynq** (Zedboard) and **Zynq UltraScale+** (ZCU102):

CPU+FPGA	Partitioning	Frames per second	
		Estimation	Real
ZedBoard	all software	18.72	22.05
	1x canny in HW	15.42	18.26
	2x canny in HW	23.25	34.6
ZCU102	all software	28.52	32.15
	1x canny in HW	21.48	24.44
	2x canny in HW	30.07	35.42
	4x canny in HW	31.14	35.75

- We have also preliminar results from **an NG-Ultra dynamic virtual platform** (estimations are located between the Zedboard and ZCU201).
- Don’t miss tomorrow paper in the session platform (fr1.4.2):

Make life easier for embedded software engineers facing complexe hardware architectures